WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

M first terminals and N second terminals, where M and N are positive integers, and where $M > N > 1$;

a converter which receives M base-A-level input signals from the M first terminals, respectively, which encodes each of A^M values represented by the M base-A-level input signals as a different base-K value represented by N base-K-level output signals, and which outputs the N base-K-level output signals to the N second terminals, respectively, where A and K are positive integers, and where $K > A > 1$.

2. The integrated circuit of claim 1, wherein the N terminals are pin terminals.

3. The integrated circuit of claim 1, further comprising a memory cell array, wherein the M terminals are coupled to the memory cell array, and wherein the N terminals are data pin terminals.

4. The integrated circuit of claim 1, further comprising a memory cell array and an address decoder coupled to the memory cell array, wherein the M terminals

are coupled to the address decoder, and wherein the N pin terminals to address pin terminals.

5. The integrated circuit of claim 1, further comprising a memory cell array and a command decoder coupled to the memory cell array, wherein the M terminals are coupled to the command decoder, and wherein the N terminals are command pin terminals.

6. The integrated circuit of claim 1, further comprising a memory cell array, and a command decoder and an address buffer coupled to the memory cell array, wherein the M terminals are coupled to at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N terminals are at least one of data pin terminals, command pin terminals and address pin terminals.

7. The integrated circuit of claim 1, wherein A = 2.

8. The integrated circuit of claim 7, wherein M = 3, N = 2 and K = 3.

9. The integrated circuit of claim 1, wherein the converter comprises:

an encoder which receives the M base-A-level input signals and which outputs at least M+1 encoded signals; and

an output buffer which receives the at least M+1 encoded signals and outputs the N base-K-level output signals.

10. The integrated circuit of claim 9, wherein A = 2, M = 3, N = 2 and K = 3.

11. An integrated circuit, comprising:

N first terminals and M second terminals, where M and N are positive integers, and where M > N > 1;

a converter which receives N base-K-level input signals from the N first terminals, respectively, which decodes each base-K value represented by the N base-K-level input signals into a different one of A^M values of M base-A-level output signals, and which outputs the M base-A-level output signals to the M second terminals, respectively, where A and K are positive integers, and where K > A > 1.

12. The integrated circuit of claim 11, wherein the N terminals are pin terminals.

13. The integrated circuit of claim 11, further comprising a memory cell array, wherein the M terminals are coupled to the memory cell array, and wherein the N terminals are data pin terminals.

14. The integrated circuit of claim 11, further comprising a memory cell array and an address decoder coupled to the memory cell array, wherein the M terminals are coupled to the address decoder, and wherein the N pin terminals are address pin terminals.

15. The integrated circuit of claim 11, further comprising a memory cell array and command decoder coupled to the memory cell array, wherein the M terminals are coupled to the command decoder, and wherein the N terminals are command pin terminals.

16. The integrated circuit of claim 11, further comprising a memory cell array, and a command decoder and an address buffer coupled to the memory cell array, wherein the M terminals are coupled to at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N terminals are at least one of data pin terminals, command pin terminals and address pin terminals.

17. The integrated circuit of claim 11, wherein A = 2.

18. The integrated circuit of claim 17, wherein M = 3, N = 2 and K = 3.

19. The integrated circuit of claim 11, wherein the converter comprises:

an input buffer which receives the N base-K-level input signals and which outputs at least M+1 coded signals; and

an decoder which receives the at least M+1 coded signals and which outputs the M base-A-level output signals.

20. The integrated circuit of claim 19, wherein A = 2, M = 3, N = 2 and K = 3.

21. An integrated circuit, comprising:

M first terminals and N second terminals, where M and N are positive integers, and where M > N > 1;

a first converter which receives M base-A-level output signals from the M first terminals, respectively, which encodes each of A^M values of the M base-A-level

output signals into a different base-K value represented by N base-K-level output signals, and which outputs the N base-K-level output signals to the N second terminals, respectively, where A and K are positive integers, and where $K > A > 1$; and

a second converter which receives N base-K-level input signals from the N first terminals, respectively, which decodes each base-K value represented by the N base-K-level input signals into a different one of A^M values of M base-A-level input signals, and which outputs the M base-A-level input signals to the M second terminals, respectively.

22. The integrated circuit of claim 21, wherein the N terminals are pin terminals.

23. The integrated circuit of claim 21, further comprising a memory cell array, wherein the M terminals are coupled to the memory cell array, and wherein the N terminals are data pin terminals.

24. The integrated circuit of claim 21, further comprising a memory cell array and an address decoder coupled to the memory cell array, wherein the M terminals

are coupled to the address decoder, and wherein the N pin terminals are address pin terminals.

25. The integrated circuit of claim 21, further comprising a memory cell array and command decoder coupled to the memory cell array, wherein the M terminals are coupled to the command decoder, and wherein the N terminals are command pin terminals.

26. The integrated circuit of claim 21, further comprising a memory cell array, and a command decoder and an address buffer coupled to the memory cell array, wherein the M terminals are coupled to at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N terminals are coupled to at least one of data pin terminals, command pin terminals and address pin terminals.

27. The integrated circuit of claim 21, wherein A = 2.

28. The integrated circuit of claim 27, wherein M = 3, N = 2 and K = 3.

29. The integrated circuit of claim 21, wherein the first converter comprises (a) an encoder which receives the M base-A-level output signals and which outputs at least M+1 encoded signals, and (b) an output buffer which receives the at least M+1 encoded signals and outputs the N base-K-level output signals; and

wherein the second converter comprises (a) an input buffer which receives the N base-K-level input signals and which outputs at least M+1 coded signals, and (b) an decoder which receives the at least M+1 coded signals and which outputs the M base-A-level input signals.

30. The integrated circuit of claim 29, wherein A = 2, M = 3, N = 2 and K = 3.

31. An integrated circuit comprising:

a memory device including an memory cell array, an address decoder and a command decoder;

a plurality of pin terminals; and

an interface circuit operatively coupled between the memory device and the plurality of pin terminals, said interface circuit comprising (a) a first converter which receives three binary-level output signals from three respective signal lines of the memory device, which encodes each of eight values represented by the three

binary-level output signals into a ternary value represented by two ternary-level output signals, and which outputs the two ternary-level output signals to two of said plurality of pin terminals, respectively, and (b) a second converter which receives two ternary-level input signals from said two pin terminals, respectively, which decodes each ternary value represented by the two ternary-level input signals into a different one of eight values represented by three binary-level input signals, and which outputs the three binary-level input signals to said three signal lines of the memory device, respectively.

32. The integrated circuit of claim 31, wherein the interface circuit is coupled between the memory cell array and the pin terminals, and wherein the pin terminals are data pin terminals.

33. The integrated circuit of claim 31, wherein the interface circuit is coupled between the address decoder and the pin terminals, and wherein the pin terminals are address pin terminals.

34. The integrated circuit of claim 31, wherein the interface circuit is coupled between the command decoder

and the pin terminals, and wherein the pin terminals are command pin terminals.

35. The integrated circuit of claim 31, wherein the first converter comprises (a) an encoder which receives the three binary-level output signals and which outputs at least four encoded signals, and (b) an output buffer which receives the at least four encoded signals and outputs the two ternary-level output signals; and

wherein the second converter comprises (a) an input buffer which receives the two ternary-level input signals and which outputs at least four coded signals, and (b) an decoder which receives the at least four coded signals and which outputs the three binary-level input signals.

36. A method of interfacing an internal circuit of an integrated circuit device with output terminals of the integrated circuit device, said method comprising:

receiving M base-A-level output signals from M terminals of the internal circuit, respectively;

encoding each of A^M values represented by the M base-A-level output signals as a different base-K value represented by N base-K-level output signals; and

outputting the N base-K-level output signals to N output terminals of the integrated circuit device, respectively,

wherein M, N, A and K are positive integers, wherein M > N > 1, and wherein K > A > 1.

37. The method of claim 36, wherein the N output terminals are pin terminals of the integrated circuit device.

38. The method of claim 37, wherein the internal circuit of the integrated circuit device is a memory cell array, and wherein the N output terminals are data pin terminals.

39. The method of claim 37, wherein the integrated circuit includes a memory cell array, and a command decoder and an address buffer coupled to the memory cell array, wherein the internal circuit is at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N output terminals are at least one of data pin terminals, command pin terminals and address pin terminals.

40. A method of interfacing an internal circuit of an integrated circuit device with input terminals of the integrated circuit device, said method comprising:

receiving N base-K-level input signals from N input terminals of the integrated circuit device, respectively;

decoding each base-K value represented by the N base-K-level input signals into a different one of A^M values of M base-A-level input signals; and

outputting the M base-A-level input signals to M terminals of the internal circuit, respectively,

wherein M, N, A and K are positive integers, wherein $M > N > 1$, and wherein $K > A > 1$.

41. The method of claim 40, wherein the N input terminals are pin terminals of the integrated circuit device.

42. The method of claim 41, wherein the internal circuit of the integrated circuit device is a memory cell array, and wherein the N input terminals are data pin terminals.

43. The method of claim 41, wherein the integrated circuit device includes a memory cell array, and a command decoder and an address buffer coupled to the

memory cell array, wherein the internal circuit is at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N input terminals are at least one of data pin terminals, command pin terminals and address pin terminals.

44. A method of interfacing an internal circuit of an integrated circuit device with input/output terminals of the integrated circuit device, said method comprising:

a first signal conversion process which comprises (a) receiving M base-A-level output signals from M terminals of the internal circuit, respectively, (b) encoding each of A^M values represented by the M base-A-level output signals as a different base-K value represented by N base-K-level output signals, and (c) outputting the N base-K-level output signals to N input/output terminals of the integrated circuit device, respectively; and

a second signal conversion process which comprises (a) receiving N base-K-level input signals from the N input/output terminals of the integrated circuit device, respectively, (b) decoding each base-K value represented by the N base-K-level input signals into a different one of A^M values of M base-A-level input signals, and (c)

outputting the M base-A-level input signals to the M terminals of the internal circuit, respectively;

wherein M, N, A and K are positive integers, wherein $M > N > 1$, and wherein $K > A > 1$.

45. The method of claim 44, wherein the N input/output terminals are pin terminals of the integrated circuit device.

46. The method of claim 45, wherein the internal circuit of the integrated circuit device is a memory cell array, and wherein the N input/output terminals are data pin terminals.

47. The method of claim 45, wherein the integrated circuit device includes a memory cell array, and a command decoder and an address buffer coupled to the memory cell array, wherein the internal circuit is at least one of the memory cell array, the command decoder, and the address buffer, and wherein the N input/output terminals are at least one of data pin terminals, command pin terminals and address pin terminals.